AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Previously Presented): A compound semiconductor device comprising:

a substrate;

a channel layer disposed above said substrate and consisting essentially of GaN;

an electron supply layer disposed above said channel layer and consisting essentially of n-type Al.sub.qGa.sub.1-qN ($0<q \leq 1$);

a cap layer disposed above said electron supply layer, having a surface, and consisting essentially of n-type GaN;

a gate electrode disposed on the surface of said cap layer and forming a Schottky contact;

recesses formed on both sides of said gate electrode on source and drain sides by removing at least part of said cap layer from the surface, said recess having a bottom surface of a roughness larger than a roughness of the surface of said cap layer under said gate electrode;

a source electrode disposed on the bottom surface of said recess on the source side; and

a drain electrode disposed on the bottom surface of said recess on the drain side.

Claim 2 (Original): The compound semiconductor device according to claim 1, wherein the roughness of the surfaces of the recesses on the source and drain sides is in a range from about 1.5 times to about 10 times the roughness of the surface of said cap layer under said gate electrode.

Claim 3 (Original): The compound semiconductor device according to claim 1, further comprising a passivation film made of insulating material and covering said cap layer and said recesses on the source and drain sides.

Claim 4 (Original): The compound semiconductor device according to claim 3, wherein a notch is formed in at least said cap layer between said gate electrode and said drain electrode, and said passivation film covers a surface of said notch.

Claim 5 (Original): The compound semiconductor device according to claim 1, wherein another notch is formed in at least said cap layer between said gate electrode and said source electrode, and said passivation film covers a surface of said another notch.

Claim 6 (Original): The compound semiconductor device according to claim 5, wherein at least one of said notch and said another notch traverses said cap layer in a depth direction and reaches an inside of said electron supply layer.

Claim 7 (Original): The compound semiconductor device according to claim 1, wherein an electron affinity ß of said cap layer is larger than an electron affinity α of said electron supply layer, $ß > α$.

Claim 8 (Original): The compound semiconductor device according to claim 1, wherein at least one of said recesses on the source and drain sides reaches an interface between said cap layer and said electron supply layer, and the surface roughness makes said cap layer partially left and said electron supply layer partially exposed.

Claim 9 (Currently Amended): The compound semiconductor device according to claim 1, wherein said channel layer, said electron supply-layer and said cap layer do not contain [[in]] In.

Claim 10 (Original): The compound semiconductor device according to claim 1, wherein said recess on the source side is deeper than said recess on the drain side.

Claim 11 (Original): A method of manufacturing a compound semiconductor device comprising the steps of: (a) epitaxially laminating above a substrate a channel layer consisting essentially of GaN, an electron supply layer consisting essentially of n-type Al.sub.qGa.sub.1-qN ($0<q \leq 1$) and a cap layer consisting essentially of n-type GaN, in this order recited; (b) forming a gate electrode on said cap layer, said gate electrode having a Schottky contact; (c) etching at least

part of the cap layer to form recesses on both sides of said gate electrode on source and drain sides, in such a manner that a bottom surfaces of said recesses have a roughness larger than a roughness of a surface of said cap layer under said gate electrode; and (d) forming a source

electrode and a drain electrode on the bottom surfaces of said recesses on the source and drain sides.

Claim 12 (Original): The method of manufacturing a compound semiconductor device according to claim 11, wherein said step (c) partially leaves said cap layer and partially exposes said electron supply layer by positively utilizing said roughness, and said step (d) forms one or both of said source and drain electrodes so as to make one or both contact both said cap layer and said electron supply layer.

Claim 13 (Original): The method of manufacturing a compound semiconductor device according to claim 11, further comprising a step of exposing the surfaces of said recesses to plasma after said step (c).

Claim 14 (Original): The method of manufacturing a compound semiconductor device according to claim 11, wherein said step (c) includes etching said recess on the source side by using a mask and etching said recess on the drain side by using another mask.

Claim 15 (Original): The method of manufacturing a compound semiconductor device according to claim 11, further comprising a step of forming a notch through said cap layer, said notch traversing in a depth direction said cap layer at least between said gate electrode and said drain electrode or between said source electrode and said gate electrode.

Claim 16 (Previously Presented): The compound semiconductor device according to claim 1, wherein said recesses are formed by removing partial depth of said cap layer.

Claim 17 (Previously Presented): The compound semiconductor device according to claim 16, wherein partial thickness of said cap layer remains between the source electrode and the electron supply layer and between the drain electrode and the electron supply layer.

Claim 18 (Previously Presented): The compound semiconductor device according to claim 1, wherein at least one of said recesses is formed by removing entire depth of said cap layer and some depth of the electron cap layer.

Claim 19 (Previously Presented): The compound semiconductor device according to claim 18, wherein both of said recesses are formed by removing entire depth of said cap layer and some depth of the electron supply layer.

Claim 20 (Previously Presented): The compound semiconductor device according to claim 3, wherein said passivation film is thinner than the source, gate, and drain electrodes.

Claim 21 (Previously Presented): The compound semiconductor device according to claim 10, wherein said cap layer remains between said drain electrode and said electron supply layer.

Claim 22 (Previously Presented): The compound semiconductor device according to claim 21, wherein said recess on the source side goes some depth in said electron supply layer.

Claim 23 (New): The compound semiconductor device according to claim 16, wherein said recesses leave said cap layer having a thickness of 2 nm or thinner under the recesses.

Claim 24 (New): The compound semiconductor device according to claim 23, wherein the cap layer establishes a lower potential barrier under the recesses than in portions of the cap layer outside the recesses.

Claim 25 (New): The compound semiconductor device according to claim 23, wherein the cap layer establishes a shorter potential barrier length under the recesses than in portions of the cap layer outside the recesses.

Claim 26 (New): The compound semiconductor device according to claim 23, wherein the cap layer has reduced piezo polarization and spontaneous polarization under the recesses than in portions of the cap layer outside the recesses.

Claim 27 (New): The compound semiconductor device according to claim 16, wherein the cap layer forms a stepping down edge at each of the recesses.

Claim 28 (New): The compound semiconductor device according to claim 27, wherein said source and drain electrodes are separated from said stepping-down edges.